



Bhattacharya 1-4-2-2-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): R. Bhattacharya et al.

Case: 1-4-2-2-1

Serial No.: 10/620,045

Filing Date: July 15, 2003

Group: To Be Assigned

Examiner: To Be Assigned

Title: Method and Apparatus for Automatic Generation of
Multiple Integrated Circuit Simulation Configuration

I hereby certify that this paper is being deposited on this date with the
U.S. Postal Service as first class mail addressed to the Commissioner for
Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature:

Date: September 3, 2003

TRANSMITTAL OF FORMAL DRAWINGS

Mail Stop PGPUB Drawings
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attention: Official Draftsperson

Sir:

Applicants submit herewith five (5) sheets of formal drawings in the above-referenced application.

Respectfully submitted,

Joseph B. Ryan
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
Attorney for Applicant(s)
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517

Date: September 3, 2003